

U.S. Department of Commerce, Patent and Trademark Office				Atty Docket No.		Application No.		
				NS-5737 US		10/803,203		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Applicant(s)		Confirmation No.		
Substitute PTO Form 1449				Bulucea, Constantin		5841		
Filing Date				Group				
17 March 2004						28112826		
U.S. Patent Documents								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
TE	AA	5,047,358	09/1991	Kosiak et al.	437	034		
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Foreign Patent Documents								
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TE	AJ	298,421 A2	05/1988	Europe	027	010		
	AK							
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
TE	AL	Appels et al., "Local Oxidation of Silicon and Its Applications in Semiconductor-Device Technology", <u>Philips Res. Rpts.</u> , vol. 25, 1970, pp. 118 - 132						
	AM	Black et al., "CMOS Process for High-performance Analog LSI", <u>IEDM Tech. Dig.</u> , 1976, pp. 331 - 334						
	AN	Bohr, "Industry-Leading Transistor Performance Demonstrated on Intel's 90-nanometer Logic Process", Intel Corp., ftp://download.intel.com/research/silicon/90nm_press_briefing-technical.pdf , 13 Aug. 2002, pp. 1 - 21						
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	AP	Brederlow et al., "Hot Carrier Degradation of the Low Frequency Noise of MOS Transistors under Analog Operating Conditions", <u>37th Ann. IEEE Int'l Rel. Phys. Symp. Procs.</u> , 23 - 25 Mar. 1999, pp. 239 - 242						
	AQ	Brown, "Trends in Advanced Process Technology-Submicrometer CMOS Device Design and Process Requirements", <u>Procs. IEEE</u> , Dec. 1986, pp. 1678 - 1702						
	AR	Bulucea et al., "Threshold Voltage Control in Buried-Channel MOSFETs", <u>Solid-State Electronics</u> , vol. 41, no. 9, 1997, pp. 1345 - 1354						
TE	AS	Chaparala et al., "NBTI in Dual Gate Oxide PMOSFETs", 2003 8th Int'l Symp. on Plasma- and Process-Induced Damage, 24 and 25 Apr. 2003, pp. 138 - 141						
Examiner <u>TE</u>			Date Considered <u>12/10/05</u>					
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.								

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		17 March 2004	Unknown 2826
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TE	BA	Chen, <u>CMOS Devices and Technology for VLSI</u> (Prentice Hall), 1990, pp. 174 - 232	
	BB	Chew et al., "Impact of 0.25 μ m Dual Gate Oxide CMOS Process on the Flicker Noise Characteristics of Multi-Fingered MOSFETs for Wireless Applications", <u>2001 Int'l Symp. VLSI Tech., Systems, and Appl'ns. Procs. Tech. Paps.</u> , 18 - 20 Apr. 2001, pp. 220 - 223	
	BC	Chew et al., "Impact of 0.25 μ m dual gate oxide thickness CMOS process on flicker noise performance of multi-fingered deep-submicron MOS devices", <u>IEEE Procs.-Circuits Devices Sys.</u> , Dec. 2001, pp. 312 - 317	
	BD	Cunningham, "CMOS Technology . . . Overcoming Yield Problems", Technology Assocs. and O.D. Trapp, 1987, pp. 9 - 22	
	BE	Davari et al., "A High Performance 0.25 μ m CMOS Technology", <u>IEDM Tech. Dig.</u> , 11 - 14 Dec. 1988, pp. 56 - 59	
	BF	El-Kareh, <u>Fundamentals of Semiconductor Processing Technologies</u> (Kluwer Acad. Pubs.), 1995, pp. 445 - 466	
	BG	Faggin et al., "Silicon Gate Technology", <u>Solid-State Electronics</u> , vol. 13, 1970, pp. 1125 - 1144	
	BH	Fujii et al., "A 45ns 16Mb DRAM with Triple-Well Structure", <u>IEEE Int'l Solid-State Circs. Conf., Dig. Tech. Paps.</u> , 1989, pp. 248, 249, and 354	
	BI	Fujii et al., "A 45-ns 16-Mbit DRAM with Triple-Well Structure", <u>IEEE J. Solid-State Circs.</u> , Oct. 1989, pp. 1170 - 1175	
	BJ	Gray et al., <u>Analysis and Design of Analog Integrated Circuits</u> (John Wiley & Sons), 1977, pp. 607 - 673	
	BK	Grove, <u>Physics and Technology of Semiconductor Devices</u> (John Wiley & Sons), 1967, pp. 108 - 110 and 342 - 345	
	BL	Hillenius et al., "Gate Material Work Function Considerations For 0.5 Micron CMOS", <u>Procs. IEEE Int'l Conf. Computer Design: VLSI in Computers</u> , 7 - 10 Oct. 1985, pp. 147 - 150	
	BM	Hu et al., "Design and Fabrication of P-channel FET for 1- μ m CMOS Technology," <u>IEDM Tech. Dig.</u> , 11 - 15 Dec. 1982, pp. 710 - 713	
	BN	Hung et al., "A 25.9-GHz Voltage-Controlled Oscillator in a CMOS Process", <u>2000 Symp. VLSI Circs., Dig. Tech Paps.</u> , 2000, pp. 100 and 101	
	BO	Hung et al., "A Fully Integrated 5.35-GHz CMOS VCO and a Prescaler", <u>2000 IEEE Radio Freq. Integ. Circs. Symp.</u> , 2000, pp. 69 - 72	
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	BQ	Kimijima et al., "Improvement of 1/f noise by using VHP (Vertical High Pressure) oxynitride gate insulator for deep-submicron RF and analog CMOS", <u>1999 Symp. VLSI Tech., Dig. Tech Paps.</u> , 1999, pp. 119 and 120	
	BR	King et al., "A Polycrystalline-Si _{1-x} Ge _x -Gate CMOS Technology", <u>IEDM Tech. Dig.</u> , 9 - 12 Dec. 1990, pp. 253 - 256	
TD	BS	Kooy et al., "Selective Oxidation of Silicon and its Device Applications", <u>Semiconductor Silicon</u> , 1973, pp. 860 - 879	
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1	CB	Lee et al., "Gate Oxide Thinning Effects at the Edge of Shallow Trench Isolation in the Dual Gate Oxide Process", 6th Int'l Conf. VLSI and CAD, 26 and 27 Oct. 1999, pp. 249 - 352	
	CC	Lee et al., <u>The Design of CMOS Radio-Frequency Integrated Circuits</u> (Cambridge Univ. Press), 1998, pp. 252 - 255	
	CD	Li et al., "A Comparison of CMOS and SiGe LNA's and Mixers for Wireless LAN Application", <u>Procs. Custom Integ. Circs. Conf.</u> , 2001, pp. 531 - 534	
	CE	Liu et al., "Multiple Gate Oxide Thickness for 2GHz System-on-A-Chip Technologies", <u>IEDM Tech. Dig.</u> , 6 - 9 Dec. 1998, pp. 589 - 592	
	CF	Meyer et al., "Integrable High Voltage CMOS: Devices, Process Application", <u>IEDM Tech. Dig.</u> , 1 - 4 Dec. 1985, pp. 732 - 735	
	CG	Mihaila et al., "Nonlinear Effects in the 1/f Noise of a 2D Electron Gas", <u>Int'l J. Chaos Theory and Appl'ns</u> , vol. 6, no. 3, 2001, pp. 47 - 55.	
	CH	Mihaila, "Image of Phonon Spectrum in the 1/f Noise of Semiconductors", <u>Procs. 1999 Int'l Semiconductor Conf.</u> , 5 - 9 Oct. 1999, pp. 117 - 120	
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	CJ	Montree et al., "Comparison of buried and surface channel PMOS devices for low voltage 0.5 μ m CMOS", 1993 Int'l Symp. VLSI Tech., Systems, and Appl'ns, <u>Procs. Tech. Paps.</u> , 12 - 14 May 1993, pp. 11 - 14	
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	CL	Muth, "Matrix Method for Latch-up Free Demonstration in a Triple-Well Bulk-Silicon Technology", <u>IEEE Trans. Nuclear Sci.</u> , vol. 39, 1992, pp. 396 - 400	
	CM	Nakahara et al., "Relief of hot carrier constraint on submicron CMOS devices by use of a buried channel structure", <u>IEDM Tech. Dig.</u> , 1 - 4 Dec. 1985, pp. 238 - 241.	
	CN	Nemirovsky et al., "1/f Noise in CMOS Transistors for Analog Applications", <u>IEEE Trans Elec. Devs.</u> , May 2001, pp. 921 - 927	
	CO	Ng, <u>Complete Guide to Semiconductor Devices</u> (McGraw-Hill), 1995, pp. 573 - 575	
	CP	Nguyen et al., "A Comparison of Buried Channel and Surface Channel MOSFETs for VLSI", <u>IEEE Trans. Elect. Devs.</u> , Oct. 1982, pp. 1663 and 1664.	
	CQ	Nishida et al., "SoC CMOS Technology for NBTI/HCI Immune I/O and Analog Circuits Implementing Surface and Buried Channel Structures", <u>IEDM Tech. Dig.</u> , 2 - 5 Dec. 2001, pp. 39.4.1 - 39.4.4	
	CR	Nishiuchi et al., "A Normally-off Type Buried Channel MOSFET for VLSI Circuits", <u>IEDM Tech. Dig.</u> , Dec. 1978, pp. 26 - 29	
	CS	O et al., "1/f Noise of NMOS and PMOS Transistors and their Implications to Design of Voltage Controlled Oscillators", 2002 IEEE Radio Freq. Integ. Circs. Symp., 2002, pp. 59 - 62	
112	CT	O et al., "CMOS Components for 802.11b Wireless LAN Applications", 2002 IEEE Radio Freq. Integ. Circs. Symp., 2002, pp. 103 - 106	
Examiner <i>thm</i>		Date Considered 12/10/05	
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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)			
<i>TE</i>	DA	O et al., "Integration of Two Different Gate Oxide Thicknesses in a 0.6- μ m Dual Voltage Mixed Signal CMOS Process", <u>IEEE Trans. Elec. Devs.</u> , Jan. 1995, pp. 190 - 192	
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	DC	Ohzone et al., "Silicon-Gate n-Well CMOS Process by Full Ion-Implantation Technology", <u>IEEE Trans Elec. Devs.</u> , Sep. 1980, pp. 1789 - 1795	
	DD	Park et al., "A Comparison of 1/f Noise of 0.25 μ m-NMOS and PMOS Transistors from Deep-subthreshold to Strong Inversion", <u>Int'l Conf. Noise in Physical Systems and 1/f Fluctuations</u> , 2002, pp. 153 - 156	
	DE	Park et al., "Body Bias Dependence of 1/f Noise in NMOS Transistors from Deep-Subthreshold to Strong Inversion", <u>IEEE Trans Elec. Devs.</u> , May 2001, pp. 999 - 1001	
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	DG	Parrillo et al., "Twin-Tub CMOS - A Technology for VLSI Circuits", <u>IEDM Tech. Dig.</u> , 8 - 10 Dec. 1980, pp. 752 - 755	
	DH	Razavi, "CMOS Technology Characterization for Analog and RF Design", <u>IEEE J. Solid-State Circs.</u> , Mar. 1999, pp. 268 - 276	
	DI	Stolk et al., "CMOS Device Optimization for Mixed-Signal Technologies", <u>IEDM Tech. Dig.</u> , 2 - 5 Dec. 2001, 4 pp.	
	DJ	Sun et al., "The Junction MOS (JMOS) Transistor - A High Speed Transistor for VLSI", <u>IEDM Tech. Dig.</u> , 8 - 10 Dec. 1980, pp. 791 - 794	
	DK	Sze, <u>VLSI Technology</u> (McGraw-Hill), 1988, pp. 272 - 279 and 316 - 319	
	DL	Taur et al., <u>Fundamentals of VLSI Devices</u> (Cambridge Univ. Press), 1998, pp. 58 - 90	
	DM	Tsividis, <u>Operation and Modeling of the MOS Transistor</u> (McGraw-Hill), 1987, pp. 409 - 444	
	DN	Vandamme et al., "1/f Noise in MOS Devices, Mobility or Number Fluctuations?", <u>IEEE Trans. Elec. Devs.</u> , Nov. 1994, pp. 1936 - 1945	
	DO	Vandamme, "Bulk and Surface 1/f Noise", <u>IEEE Trans. Elec. Devs.</u> , May 1989, pp. 987 - 992	
	DP	Wanlass et al., "Nanowatt Logic Using Field-Effect Metal-Oxide Semiconductor Triodes", <u>ISSCC Dig. Tech. Paps.</u> , 1963, pp. 32 and 33	
	DQ	Wong et al., "Doping of n+ and p+ Polysilicon in a Dual-gate CMOS Process", <u>IEDM Tech. Dig.</u> , 11 - 14 Dec. 1988, pp. 238 - 241	
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